REMARKS

Claims 15-19 were pending, and stood rejected. Claims 1-14 previously had been cancelled.

Claims 15-19 are cancelled hereby. New claims 20-38 are added, and are submitted to be free of deficiencies of the sort, i.e., 35 U.S.C. 112 deficiencies, that the Examiner found in the now-cancelled claims 15-19.

An Information Disclosure Statement is submitted herewith, along with the required fee of $180.

A three month extension of time to respond to the Office Action is requested, and the appropriate fee also is submitted herewith.

The new claims 20-38 are well supported by the specification, and do not introduce new matter. As non-limiting examples, representative claims are reproduced below with annotations to the exemplary embodiments of the specification.

20. (New) A switching fabric **[#102 in Figs. 1-3A, ¶ 0073]** for a network switch **[#100 in Fig. 1]**, the network switch for a switching packets in a network **[¶¶ 0003, 0078-79]**, the switching fabric comprising:

a first integrated circuit chip [**#202A in Figs. 2, ¶¶ 0080, 0131]**;

a plurality of full duplex serial links **[# 204 in Fig. 2, ¶¶ 0068, 0085]**;

a plurality of blades **[#104 in Figs. 1-3A, ¶¶ 0078, 0087]** each comprising at least one physical port **[#108 in Fig. 1, ¶¶ 0078]**, wherein each of the plurality of blades **[#104]** is coupled to the first integrated circuit chip [**#202A]** through at least one of the serial links **[# 204]**, whereby the plurality of blades are interconnected **[¶¶ 0068-69]**;

wherein the first integrated circuit chip **[#202A]** is operable to serially transmit **[#580 in Fig. 5, ¶¶ 0096, 0100]** a serial block of data **[the "serial block" is the L0-L3 portion of cycle 1 in Fig. 15A, ¶¶ 0096]** via a said serial link **[# 204]** to any of said blades **[#104]**, the serial block of data comprising originating blade identifier information **[under category of "state information" in Fig. 15A, "source slot number for crosspoint switch to BIA direction" in Fig. 15B, and "originating slot identifier information" in ¶ 0138]** and at least one byte **[D0 of Fig. 15A, ¶ 0124]** of a said packet.

21. (New) The switching fabric of claim 20, further comprising a plurality of the first integrated circuit chips **[202A-202E in Fig. 2]**, wherein each of the plurality of blades **[104A-H in Fig. 2]** is coupled to each of the plurality of first

integrated circuit chips **[202A-202E in Fig. 2]** through at least one of the plurality of serial links [**204 in Fig. 2]**, whereby the plurality of blades are interconnected.

22. (New) The switching fabric of claim 20, wherein the serial block of data further comprises an identifier of a start of a said packet **[SOP in ¶ 0123]**.

23. (New) The switching fabric of claim 20, wherein the serial block of data further comprises an identifier of an end of a said packet **[K1 in ¶ 0123 and Fig. 15C]**.

24. (New) The switching fabric of claim 20, wherein the serial block of data further comprises payload state information **["STATE" in Figs. 15A and 15B and ¶ 0123]**.

26. (New) A switching fabric **[#102 in Figs. 1-3A, ¶ 0073]** for a network switch **[#100 in Fig. 1]**, the network switch for a switching packets in a network **[¶¶ 0003, 0078-79]**, the switching fabric comprising:

a plurality of first integrated circuit chips **[202A-202E in Fig. 2, ¶¶ 0080, 0131]**; and

a plurality of blades **[#104 in Figs. 1-3A, ¶¶ 0078, 0087]** each comprising at least one physical port **[#108 in Fig. 1, ¶¶ 0078]**;

wherein each said blade **[#104]** comprises a second integrated circuit chip **[#302 in Fig. 3A, ¶¶ 0087, #600 in Fig. 6, ¶¶ 0087**, each said second integrated circuit chip **[#302, #600]** being coupled to each said first integrated circuit chip by a full-duplex serial link **[# 204 in Fig. 2, ¶¶ 0068, 0085]**, whereby the plurality of blades are interconnected **[¶¶ 0068-69]**;

wherein each said first integrated circuit is operable to serially receive **[¶¶ 0131]** a block of data **[the "block" is the L0-L3 portion of cycle 1 in Fig. 15A, ¶¶ 0096]** from a said second integrated circuit **[#302]** of a first said blade **[#104]** via a said serial link **[204]**, the block of data comprising in-band control information **[K0 in Fig. 15A, ¶¶ 0081, 0122]** and at least one byte of a said packet **[D0 of Fig. 15A, ¶ 0124]**, and to serially transmit **[#580 in Fig. 5, ¶¶ 0096, 0100]** the block of data to a said second integrated circuit **[#302]** of another said blade via another said serial link.

Similar terms in the remaining claims are similarly supported, but in the interests of brevity are omitted. If the Examiner wishes to have this support spelled out as above for each of the claims, the Examiner is requested to telephone the undersigned at (408) 207-1323, whereupon the undersigned will submit such further remarks.

Please direct questions or comments to the undersigned at (408) 207-1323.

Respectfully submitted,

Customer No.: 33,707

James E. Parsons
Attorney for Applicants
Reg. No. 34,691

I hereby certify that this correspondence is being deposited with the United States Postal Service as FIRST CLASS MAIL in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on July 12, 2006.

July 12, 2006 Debra Walker

Date Signature: Debra Walker